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# (54) Decision-feedback QPSK demodulator

(57) A QPSK demodulator for recovering a carrier signal and demodulating a QPSK data signal. The input phase modulated signal 100 is multiplied 101, 103 with a regenerated carrier signal to produce in-phase and quadrature signals (I, Q). Inverse signals ($\overline{I}$, $\overline{Q}$) are additionally formed by inverters 106, 107. Each of signals (I, $\overline{I}$, Q, $\overline{Q}$) is compared in respective voltage comparators 116-119 with a reference 120, and the comparator outputs control switches 112-115 so that the proper phase error signal is selected to control a voltage-controlled oscillator 139. If the comparator outputs are detected 130 as overlapping, the control of switches 112-115 is inhibited 132-135 and a fixed potential 137 is applied to the loop filter 138, so that a guarding signal is inserted between phase segments for fast acquisition. Finally, a demodulator for a differentially encoded QPSK signal applying the same invention with an additional translation means comparing relative change of phase is also disclosed.

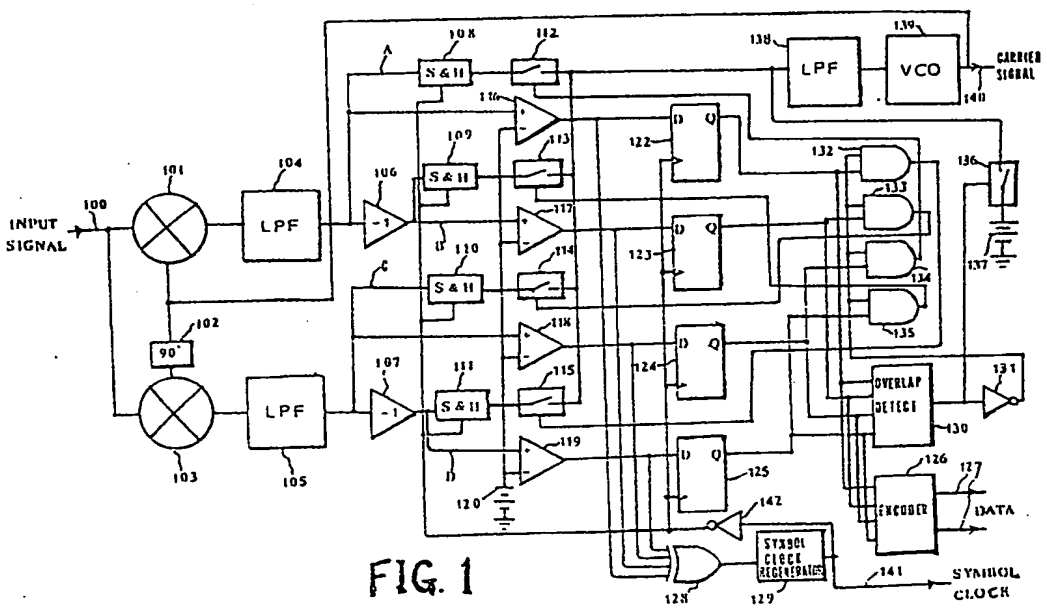


FIG. 1



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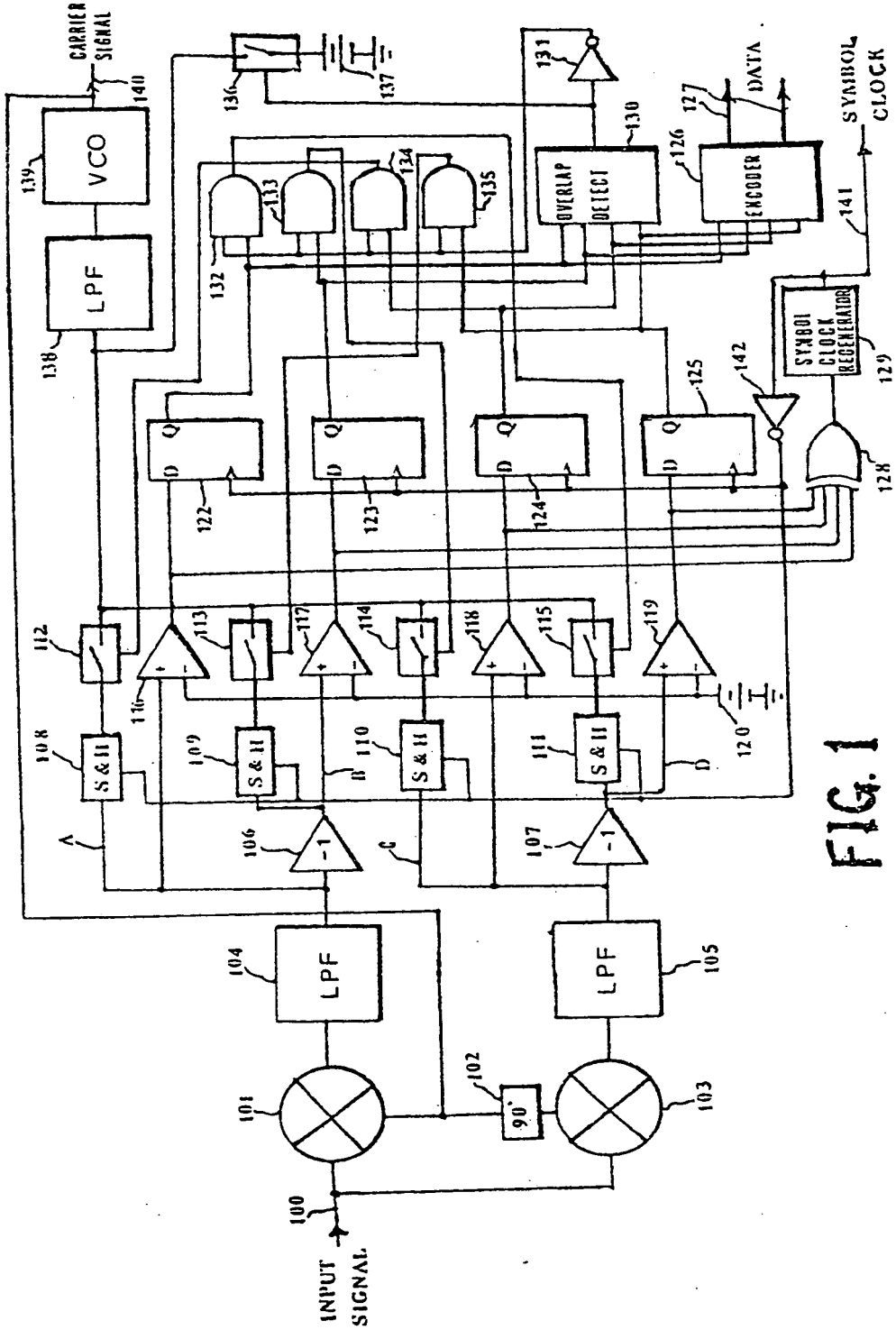

CARRIER SIGNAL
VCO
LPF
OVERLAP DETECT
ENCODER
DATA
SYMBOL CLOCK
SYMBOL CLOCK REGENERATOR
S & H
INPUT SIGNAL
90°
-1

FIG. 1

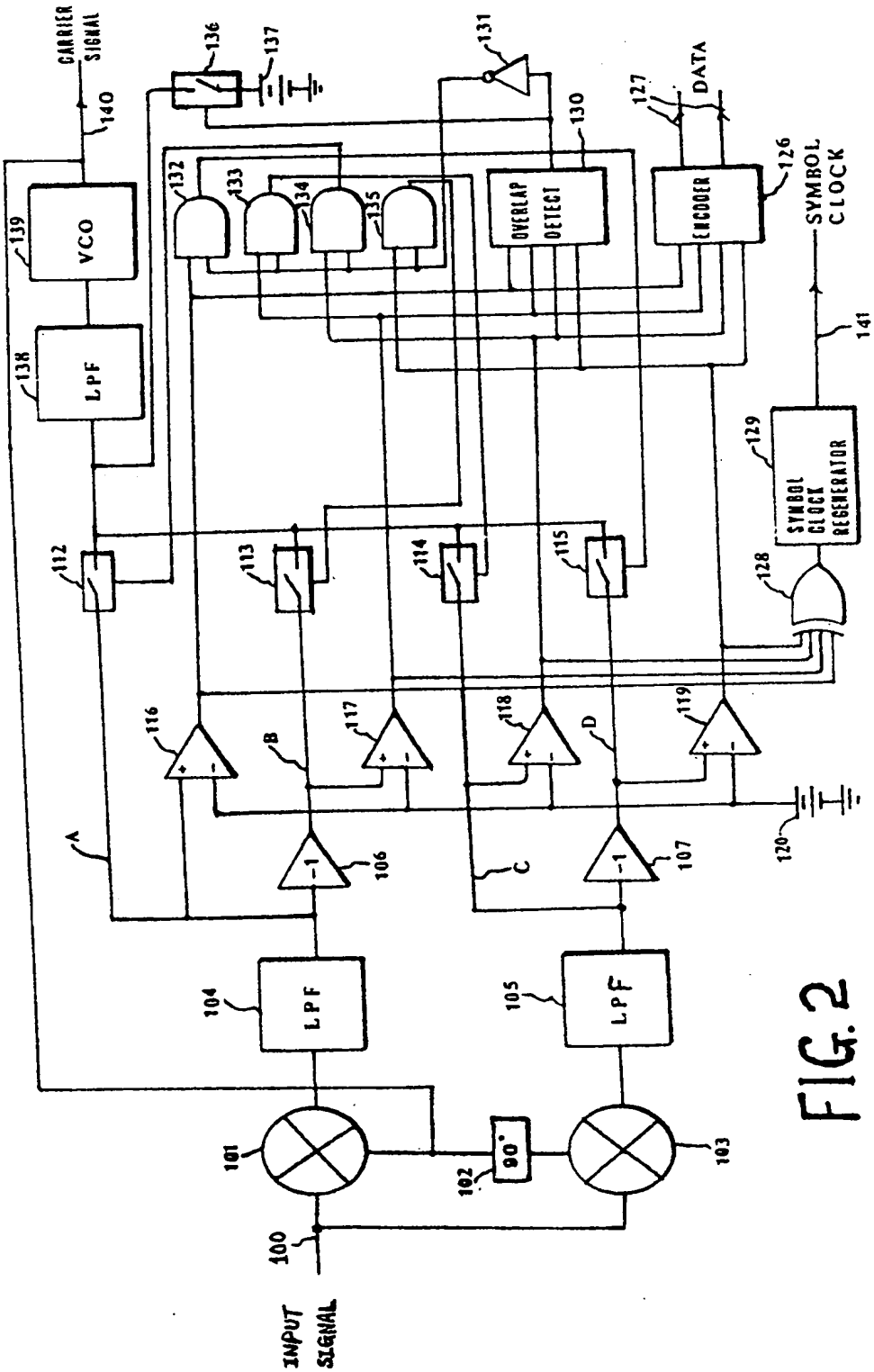

CARRIER SIGNAL
140
136
137
131
127
DATA
130
132
133
134
135
OVERLAP DETECT
126
ENCODER
SYMBOL CLOCK
139
VCO
138
LPF
141
129
SYMBOL CLOCK REGENERATOR
112
113
114
115
128
116
117
118
119
A
B
C
D
120
-1
106
-1
107
104
LPF
105
LPF
101
102
90°
103
100
INPUT SIGNAL

FIG. 2

| PHASE MODULATED INPUT | A | B | C | D |
|---|---|---|---|---|
| 0° | COS θ | -COS θ | SIN θ | -SIN θ |
| 90° | -SIN θ | SIN θ | COS θ | -COS θ |
| 180° | -COS θ | COS θ | -SIN θ | SIN θ |
| 270° | SIN θ | -SIN θ | -COS θ | COS θ |

θ = PHASE ERROR ANGLE

FIG. 3

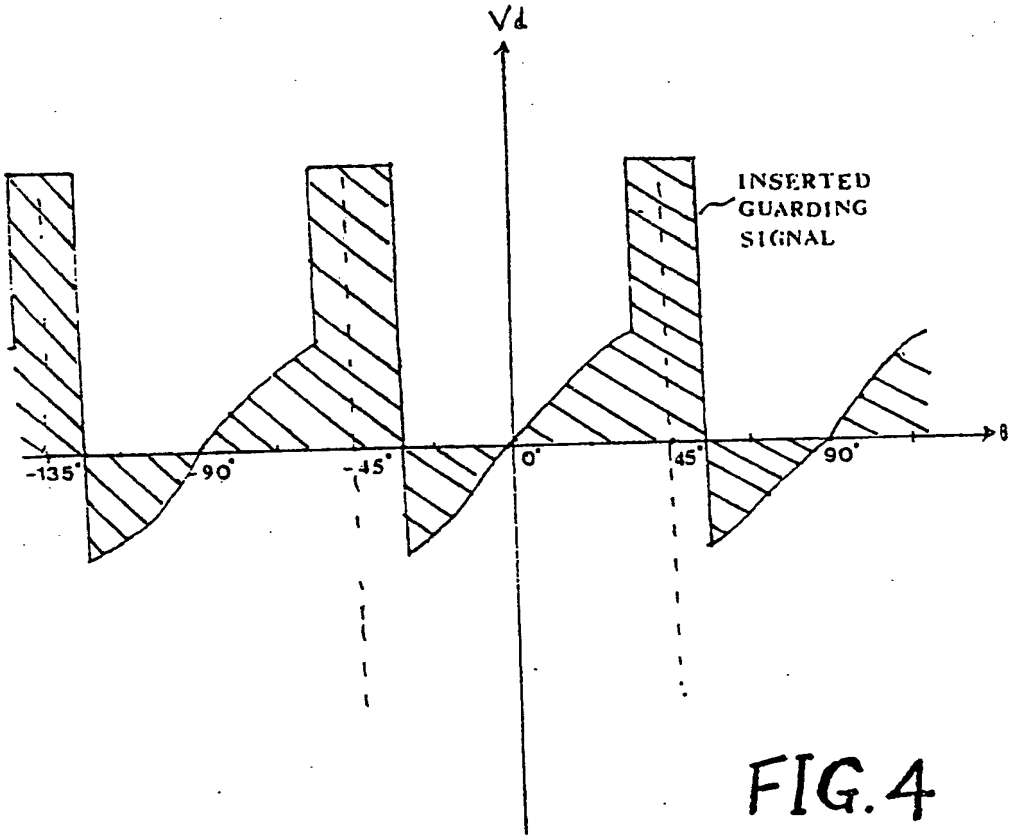



FIG. 4

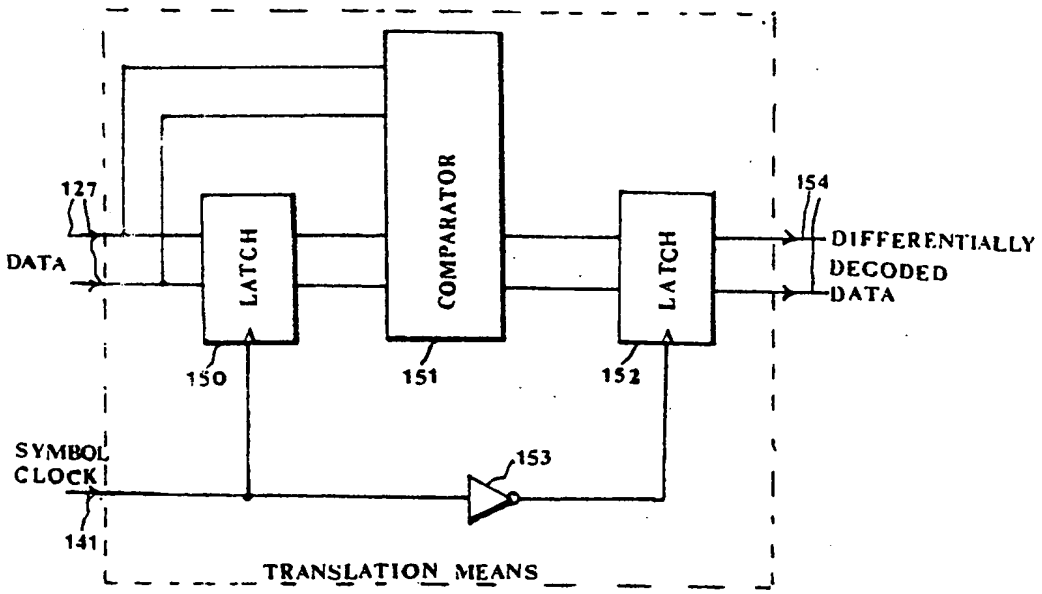
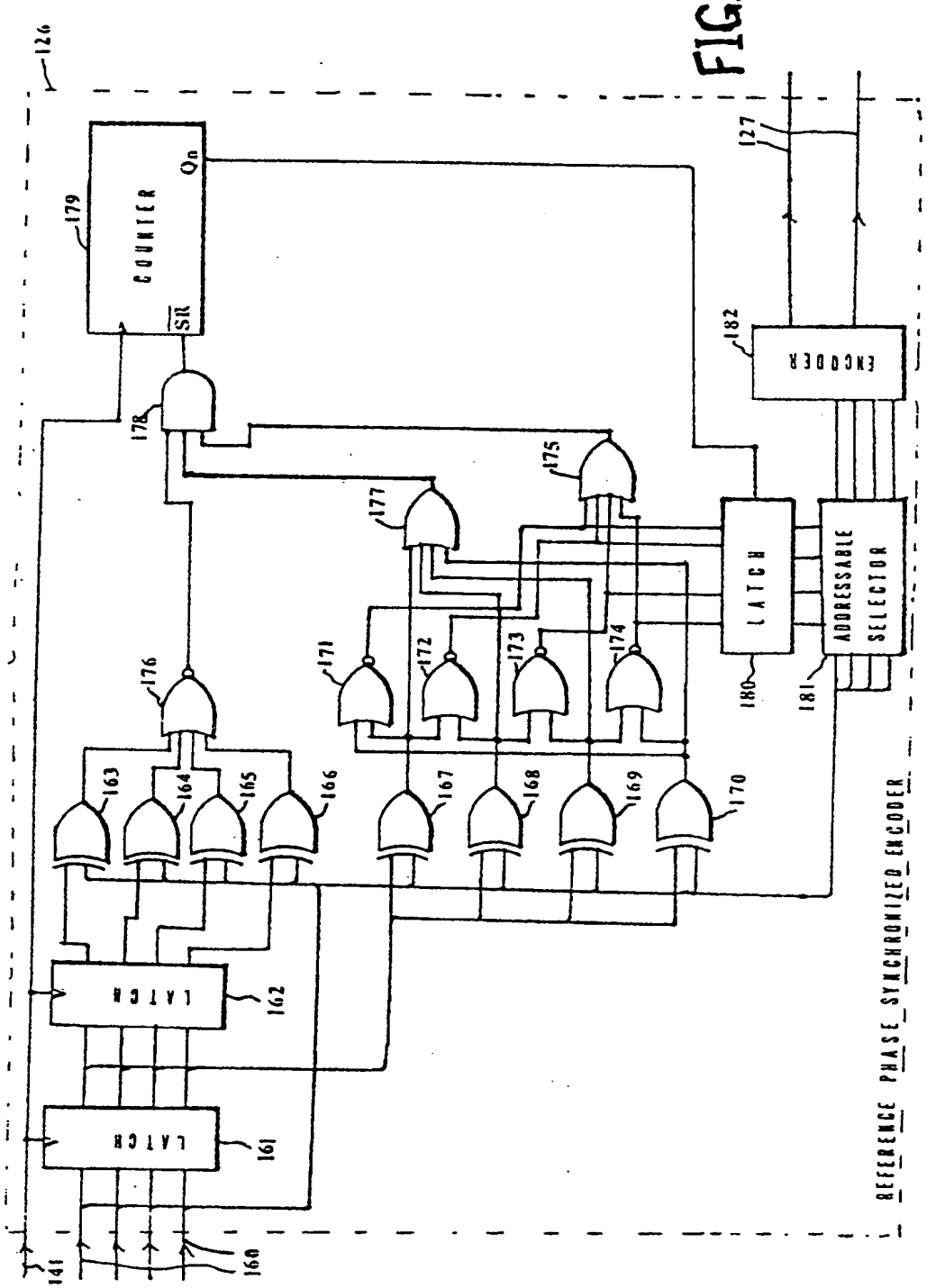

127
DATA
LATCH
COMPARATOR
LATCH
154
DIFFERENTIALLY
DECODED
DATA
150
151
152
SYMBOL
CLOCK
153
141
TRANSLATION MEANS

FIG.5

FIG.6


126
COUNTER
179
Qn
SR
127
182
ENCODER
178
175
177
LATCH
ADDRESSABLE SELECTOR
180
181
176
171
172
173
174
163
164
165
166
167
168
169
170
LATCH
162
LATCH
161
141
160
REFERENCE PHASE SYNCHRONIZED ENCODER

SPECIFICATION

**Decision-feedback QPSK demodulator**

*Background of the invention*

The present invention relates to a QPSK (quadrature phase shift keying) demodulator, and more particularly to a PSK demodulator having a decision-feedback aided carrier signal reproducing circuit.

Conventionally, Costas loops, IQ loops and decision-feedback or directed loops are popularly used for a PSK demodulator especially for N-phase signal. However, most circuits excluding their complexity have certain different disadvantages. Major problems are such as power imbalance between I and Q branches, long period of acquisition and offset voltage after a long chain of D.C. multiplications and additions. A four-phase Costas loop is shown in figure 11.9 of test "Phaselock Techniques". It applies hard limiters to determine directions of error signals. However, it may have wrong threshold decision if the phase error signal is at the mid-point. Otherwise, some phase error signals of particular phase segments have to be disregarded. A carrier recovery for M-ary PSK using a decision feedback PLL is shown in figure 4.2.37 of text 'Digital Communication". It applies a phase estimator to justify the phase error based on signals from I and Q branches. The estimated phase error further guards the direction of the I and Q branches' error signals. This type of loop requires a long acquisition time and not suitable for banks of messages with gaps in between. The arc tangent phase estimator is not practical implemented. Many stages of multiplications and additions may generate a large offset voltage.

*Summary of the invention*

In accordance with this invention, there is provided a QPSK demodulator comprising a means for reproducing a carrier signal, a means for demodulating the data, a means for reproducing the symbol clock and means for aiding acquisition.

It is an objective of this invention to prevent any imbalance problem which is common to most IQ or Costas loops and the requirement of scrambling of input data.

It is an objective of this invention to eleminate any special phase error estimate or arc tangent circuit requirement.

It is an objective of this invention to prevent the application of hard limiter having two states output guarding the decision direction which may have wrong threshold decision if the phase error signal is close to mid-point.

It is an objective of this invention to provide no requirement of any static phase shift (such as 45 degrees) which may degrade the demodulation's error rate.

It is an objective of this invention to provide no requirement of multiplication or addition between I and Q branches' signals and to have a lower value of harmonic signals, cross products, offset voltage and noise induced to the phase error signal.

It is an objective of this invention to memorize last latched frequency value during nil signal input. When the signal appears again, a long period of acquisition is not required. It is especially important for a half-plex band-band communication or mobile communication with fading blanking periods in between.

Basically, the invention applies the demodulated data to select rather than suming or multiplying the proper phase error signal to control the voltage controlled oscillator. If there is no input signal, all selectors are disabled and the last control voltage is latched to generate a stable almost same frequency for a long period of time. If there is new input signal arriving again, the loop has to compensate any slight drift of phase and frequency only which is fast in action. If the loop is in initial acquisition or out of lock condition, a fixed source of control signal is inserted between regions of phase segments as a guarding signal to prevent phase-segment sliping to many cycles and to expect a fast acquisition due to its non-linear limit band-band action.

*Brief description of the drawings*

The invention will be further described in conjunction with the accompanying drawings, which illustrate preferred and examplary embodiments, and wherein:

*Figure 1* is a diagram, partly in block form and partly in schematic showing the QPSK demodulator circuit.

*Figure 2* is a schematic of another embodiment of QPSK demodulator circuit.

*Figure 3* is a table showing phase signals relationship.

*Figure 4* is a phase error relation diagram.

*Figure 5* is a schematic of an embodiment of a translation means, and

*Figure 6* is a schematic of a reference phase synchronized encoder.

*Detailed description of the preferred embodiments*

Figure 1 illustrates a preferred embodiment of a decision-feedback QPSK demodulator. A phase modulation signal source is received at line 100 and fed to inputs of multipliers 101 and 103. The carrier signal on line 140 from voltage controlled oscillator VCO 139 is applied to other inputs of multipliers 101 and 103 via 90 degrees phase shifter 102. The output of multiplier 101 as in-phase signal is filtered by low pass filter 104 and the output of multiplier 105 as quadrature signal is filtered by low pass filter 105. Filters 104 and 105 may be a type of integrate-and-dump filter. The output of low pass filter 104 is connected to inputs of sample and hold 108, voltage comparator 116 and voltage inverter 106. The output of voltage inverter 106 is connected to inputs of sample and hold 109 and voltage comparator 117. The output of low pass filter 105 is connected to inputs of sample and hold 110, voltage comparator 118 and voltage inverter 107. The output of voltage inverter 107 is connected to inputs of sample and hold 111 and voltage comparator 119. A potential source 120 is

connected to other inputs of voltage compatators 116, 117, 118 and 119. Outputs of sample and holds 108, 109, 110 and 11 are connected to inputs of switches 112, 113, 114 and 115 correspondingly. Outputs of switches 112, 113, 114 and 115 are jointed to an input of low pass filter 138. Output of low pass filter 138 is fed to control input of VCO 139 which produces the carrier signal. Digital outputs of voltage comparators 116, 117, 118 and 119 are connected to data D inputs of flip flops 122, 123, 124 and 125 and inputs of EXCLUSIVE-OR gate 128. Outputs of flip flops 122, 123, 124 and 125 are connected to inputs of OVERLAP DETECT 130 and ENCODER 126. The output of OVERLAP DETECT 130 which indicates the relative phase error signal exists certain level enables a fixed potential source 137 applying to input of low pass filter 138 via switch 136. The inverted output via inverter 131 disables all outputs of AND gates 132, 133, 134 and 135 and indirectly opens switches 112, 113, 114 and 115. If the output of OVERLAP DETECT 130 is low, the output of flip flop 122 is fed to conduct switch 115 via AND gate 132. The output of flip flop 123 is fed to conduct switch 114 via AND gate 133. The output of flip flop 124 is fed to conduct switch 112 via AND gate 134. The output of flip flop 125 is fed to conduct switch 113 via AND gate 135. Outputs of encoder 126 are two parallel binary data outputs at line 127. Synchronization of reference phase applying preamble or frames is done externally. The application of differentially encoded QPSK input which does not require reference phase synchronization will also be described later. The output of EXCLUSIVE-OR gate 128 is connected to input of symbol clock regenerator 129 to produce symbol clock at line 141 which is fed to control inputs of sample and holds 108, 109, 110 and 111 and clock inputs of flip flops 122, 123, 124 and 125 via inverter 142.

In operation, the phase modulated signal multiplied by the regenerated carrier signal and its quadrature version to produce phase error signals at outputs of filters 104 and 105 and inverted ones at outputs of inverters 106 and 107. During steady state, they are representing SIN $\theta$, $-$SIN $\theta$, COS $\theta$ and $-$COS $\theta$ components of error signal where $\theta$ equals to phase error angle between input and carrier signals. Signals relationship is shown in Figure 3. These four signals are sampled and held at the middle of symbol clock. They are also level compared with a potential source to produce coherent detected output as high signal. The high signal which is also sampled by inverted symbol clock and appears at one output of digital latches 122, 123, 124 and 125 is used to selected proper one of switches 112, 113, 114 or 115 routing SIN $\theta$ (approxmate phase error) to input of low pass filter 138. The selection of switch accords that the coherent detected signal is 90 degrees laging to the phase error signal input. Then the sampled coherent detected output is multiplex back to two parallel data outputs. On the other hand, outputs of voltage comparators are exclusive ored to form a chain of edge signals which is used to regenerate the symbol clock at line 141. Symbol clock regenerator 129 may be a type of maximum likelihood tracker, early-late gate or a suppressed carrier recovery system described in my other Canadian application 400,188. The data clock is fed back to clock inputs of sample and holds 108, 109, 110, 111 and latches 122, 123, 124, 125. When there is nil signal input, outputs of multipliers 101 and 103 are close to zero and thus there is no output high signal detected at any voltage comparator and digital latch. As a result, switches 112, 113, 114 and 115 are disabled and their common output is disconnected from any phase error signal. The input of low pass filter 138 is in floating state and latches last acquired control voltage to generate a steady frequency output from VCO 139.

During initial acquisition or out of lock conditions, both outputs of low pass filters 104 and 105 may exist the threshold limit of potential source 120 and thus there may be two outputs of voltage comparators high at same time. OVERLAP DETECT 130 senses this condition and outputs a signal to disable any phase error signal input and enable a fixed potential source to input of low pass filter 138 as a guarding signal between phase segments. It intends to limit the acquistion's phase range within a phase segment and thus a fast acquisition is expected. A phase error diagram is shown in Figure 4. If the acquisition is nearly completed, there will be no overlaping between comparators' outputs. The demodulator functions in steady state as described.

Another embodiment with simplier circuit is shown in Figure 2. It appears as a modified Costas decision-directed loop. It eliminates the application of sample and hold and digital latches as shown in Figure 1. However, the performance is slightly degraded due to phase jitter, and filtered envelope wave-form dependance (related to data pattern).

Most descriptions of circuit connections in Figure 2 are same as Figure 1 and not repeated here. Inputs of switches 112, 113, 114 and 115 are supplied from outputs of low pass filter 104, inverter 106, low pass filter 105 and inverter 107 correspondingly. Outputs of voltage comparators are connected to inputs of OVERLAP 130, ENCODER 126 and EXCLUSIVE OR gate 128. In particular, the output of comparator 116 is applied to control input of switch 115, the output of comparator 117 is applied to control input of switch 114, the output of comparator 118 is applied to control input of switch 112 and the output of comparator 119 is applied to control input of switch 113.

In operation, the circuits function similar to first embodiment except that the input phase error signals are not sampled and not delayed for a symbol bit period. The duration of direction signal and relative position of selected phase error signal depends on the demodulated waveform which may have slight difference of delay and transient response between I and Q branches.

Two embodiments of the invention have been described. On the hand, most circuit forms stated can be implemented in digital means for easy circuit integration. For that case, analog multipliers 101 and 103 can replace by digital multipliers with

analog-to-digital inputs. Low pass filters can be replaced by digital filters. Sample and holds can be replaced by registers. Comparators and voltage inverters can be replaced by digital comparators. Switches can be replaced by logic gates. Voltage controlled oscillator can be replaced by digital controlled oscillator such as a programmable counter with SIN and COS mapped functions outputs.

The invention can be modified slightly to accept other forms of phase modulation input. The obvious one is differentially encoded QPSK modulation. For that application, an input signal source with differentially encoded QPSK is required. A translation means monitors the binary output of the demodulator, compares relative phase change for every symbol period and translate it to a decoded binary data.

Figure 5 illustrates a preferred embodiment of a translation means which accepts the binary encoded data from lines 127 of Figures 1 and 2 and translate into a differentially decoded data. The binary data is received at lines 127 and fed to inputs of latch 150 and comparator 151. The symbol clock at line 141 is fed to clock inputs of latch 150 and also of latch 152 via inverter 153. The outputs of latch 150 which are one clock period delayed version of data from lines 127 are fed to other inputs of comparator 151. The compared results from comparator 151 are sampled at latch 152 to produce the differentially decoded data at its output.

Figure 6 illustrates a preferred embodiment of a reference phase synchronized encoder which may replace encoder 126 in Figure 1 or 2. Conventionally, the reference phase synchronization is obtained by pulling the carrier recovery loop during preamble period. In this invention, the reference phase may be adjusted by modulating the encoder with an extracted ratio obtained during preamble period.

Signals at lines 160 which are digital outputs of flip flops 122 to 125 in Figure 1 or comparators 116 to 119 in Figure 2 are connected to inputs of latch 161, Exclusive-Or gates 163-170 and addressable selector 181 as shown in diagram. Outputs of latch 161 are connected to inputs of latch 162 and Exclusive-Or gates 167-170. Outputs of latch 162 are connected to inputs of Exclusive-Or gates 163-166. Outputs of Exclusive-Or gates 163-166 are collected to inputs of NOR gate 176. Outputs of Exclusive-Or gates 167-170 are fed to inputs of Or gate 177 and NOR gates 171-174 with connections as shown. Outputs of NOR gates 171-174 are collected to inputs of OR gate 175 and inputs of latch 180. Outputs of NOR gate 176, OR gate 177 and OR gate 175 are connected to inputs of AND gate 178 and its output is fed to $\overline{S}R$ synchronous reset input of counter 179. The symbol clock signal at line 141 is fed to clock inputs of latch 161, 162 and counter 179. The Qn output of counter 179 is connected to clock input of latch 180. Outputs of latch 180 are fed to addressable selector 181 as the address control. The redirected outputs of addressable selector 181 are fed to encoder 182 to form binary encoded data at lines 127.

During the preamble period and the locking of input signal being completed, a chain of repeating adjacent alternating decoded digital outpus of expected at signal lines 160. Exclusive-Or gates 163-166 compares signals at line 160 and two clocks delayed version to verify repeating of every two symbols with the result indicated at NOR gate 176's output. Exclusive-Or gates 167-170 compares signals at lines 160 and one clock delayed version to verify the signal being alternating for every symbol period with the result indicated at OR gate 177's output. NOR gates 171-174 validates the alternating symbols being adjacent to each other with the result indicated at the output of OR gate 175. The summation of informations representing a repeating alternative adjacent symbols is collected at AND gate 178 to generate an output enabling counter 179. Counter 179 acts as a time-filter to gaurantee minimum length of preamble in order to prevent any false triggering. Outputs of NOR gates 171-174 which also include the information of the relative position of the reference phase are latched at latch 180 by the output of counter 179.

Outputs of latch 180 which is kept latched after the preamble period are considered as the address control of addressable selector 181 to redirect signal lines 160 to its corresponding outputs. Thus the reference phase is adjusted depending the address applied to selector 181. The outputs of selector 181 are further encoded into binary data at lines 127 via encoder 182.

It will be apparent to those skilled in the art that changes can be made in these embodiments without department from the principles and spirit of the invention, the scope of which is defined in the appended claims. One of the obvious alternative is the replacement of loop's filter by a type of adaptive filter if the input signal is over-filtered in the channel and the nil requirement of scrambling of input data or non-sensitive to pattern variation property stated in the disclosure is preseved.

## CLAIMS

1. A decision-feedback QPSK demodulator comprising:

a) a first multiplier for producing product signals of input signal and a regenerated carrier signal,

b) a second multiplier for producing product signals of input signal and a 90 degrees phase shifted regenerated carrier signal,

c) a first low pass filter responsive to receive said product signals from first multiplier for producing a filtered in-phase signal,

d) a second low pass filter responsive to receive said product signals from second multiplier for producing a filtered quadrature signal,

e) a first voltage inverter for inverting the said in-phase signal to a negative in-phase signal,

f) a second voltage inverter for inverting said quadrature signal to a negative quadrature signal,

g) sample and hold means responsive to sample said in-phase, negative in-phase, quadrature and negative quadrature signals at the middle of later defined symbol clock signal for holding said signals at outputs of a symbol clock period,

h) voltage comparators responsive to compare said in-phase, negative in-phase, quadrature and negative quadrature signals with a potential source for having digital output signals,

i) digital latches responsive to synchronize ditigal output signals from said voltage comparators with inverted symbol clock for producing synchronized digital output signals,

j) an encoder responsive to multiplex said synchronized digital output signals for producing parallel binary data outputs,

k) switches responsive to receive output signals from said sample and hold means and be enabled by said synchronized digital output signals for passing the selected phase error signal,

l) a carrier loop's low pass filter responsive to receive the jointed output which being the selected phase error signal from said switches for producing a filtered error compensation signal,

m) a voltage controlled oscillator responsive to receive said filtered error compensation signal from said carrier loop's filter for generating a carrier signal,

n) an exclusive-or gate responsive to receive digital signals from said voltage comparators' outputs for generating a chain of non-overlating edge signals, and

o) a symbol clock regenerator responsive to receive the edge signal from said exclusive-or gate's output for regenerating a symbol clock source.

2. A decision-feedback QPSK demodulator as defined in claim 1 further comprising:

a) means for detecting no output from said voltage comparators, disabling all said switches, and floating input of said carrier loop's low pass filter if the input signal being nil, and

b) said carrier loop's filter for latching the last filtered error compensation signal and said voltage controlled oscillator for generating same carrier signal as before.

3. A decision-feedback QPSK demodulator according to claim 1, wherein said first and second low pass filters may be a type of integrate-and-dump filter synchronized by said symbol clock signal.

4. A decision-feedback QPSK demodulator according to claim 1, wherein said output from any voltage comparator is high representing the input of that particular comparator being coherent detected and the sampled output of that voltage comparator is fed to enable a switch having expected phase error signal input in order to complete the decision-feedback action.

5. A decision-feedback QPSK demodulator according to claim 1 or 4, wherein said coherent detected signal sensed by said voltage comparator's output is 90 degrees laging to said expected error signal. A proper switch is thus selected according to this relation.

6. A decision-feedback QPSK demodulator according to claim 1 or 3 wherein outputs of first and second low pass filters are sampled at the middle of symbol clock to preserve accurate phase difference signals and decision of direction even with large jitter of phase signal input.

7. A decision-feedback QPSK demodulator as defined in claim 1 further comprising overlap detect means responsive for monitoring any time overlaping outputs from said digital latches' outputs which representing a large phase error detected, disabling any phase error signal input and enabling a fixed potential source to input of said carrier loop's low pass filter.

8. A overlap detect means as defined in claim 7, wherein said enabled fixed potential source acts as a guarding signal between phase segments, intends to limit the acquisition's phase range and expects a fast acquisition under most conditions.

9. A decision-feedback QPSK demodulator comprising:

a) a first multiplier for producing product signals of input signal and a regenerated carrier signal,

b) a second multiplier for producing product signals of input signal and a 90 degrees phase shifted regenerated carrier signal,

c) a first low pass filter responsive to receive said product signals from first multiplier for producing a filtered in-phase signal,

d) a second low pass filter responsive to receive said product signals from second multiplier for producing a filtered quadrature signal,

e) a first voltage inverter for inverting the said in-phase signal to a negative in-phase signal,

f) a second voltage inverter for inverting the said quadrature signal to a negative quadrature signal,

g) voltage comparators responsive to compare said in-phase, negative in-phase, quadrature and negative quadrature signals with a potential source for having digital output signals,

h) encoder responsive to multiplex said voltage compared digital output signals for producing parallel binary data outputs,

i) switches responsive to receive output signals from said sample and hold digital means and be enabled by outputs of said voltage comparators for passing the selected phase error signal,

j) a carrier loop's low pass filter responsive to receive the jointed output form said switches which being the selected phase error signal for producing a filtered error compensation signal,

k) a voltage controlled oscillator responsive to receive said filtered error compensation signal from said carrier loop's filter for generating a carrier signal,

l) an exclusive-or gate responsive to collect digital signals from said voltage comparators' outputs for generating a chain of non-overlaping edge signals, and

m) a symbol clock regenerator responsive to recieve the edge signal from said exclusive-or gate's output for regenerating a symbol clock source.

10. A decision-feedback QPSK demodulator as defined in claim 9 further comprising:

a) means for detecting no output from said voltage comparators, disabling all said switches, and floating input of said carrier loop's low pass filter if the input signal being nil, and

b) said carrier loop's filter for latching the last filtered error compensation signal and said voltage controlled oscillator for generating same carrier

signal as before.

11. A decision-feedback QPSK demodulator according to claim 9, wherein said output form any voltage comparator is high representing the input of that particular comparator being coherent detected and fed to enable a switch having expected phase error signal input in order to complete the decision-feedback action.

12. A decision-feedback QPSK demodulator according to claim 9 or 11, wherein said coherent detected signal sensed by said voltage comparator's output is 90 degrees laging to said expected error signal. A proper switch is thus selected according to this relation.

13. A decision-feedback QPSK demodulator as defined in claim 9 further comprising overlap detect means responsive for monitoring any time overlapping outputs from said voltage comparators' outputs which representing a large phase error detected, disabling any phase error signal input and enabling a fixed potential source to input of said carrier loop's low pass filter.

14. A overlap detect means as defined in claim 13, wherein said enabled fixed potential source acts as a guarding signal between phase segments, intends to limit the acquisition's phase range and expects a fast acquisition under most conditions.

15. A digital decision-feedback QPSK demodulator comprising:

a) a first digital multiplier with analog-to-digital input for producting product signals of input signal and a digital SIN output of a digital controlled oscillator,

b) a second digital multiplier with analog-to-digital input for producing product signals of input signal and a digital COS output of a digital controlled oscillator,

c) a first digital low pass filter responsive to receive said product signals from first digital multiplier for producing filtered in-phase and negative in-phase digital signals,

d) a second digital low pass filter responsive to receive said product signals from second digital multiplier for producing filtered quadrature and negative quadrature digital signals,

e) registers responsive to sample said in-phase, negative in-phase, quadrature, and negative quadrature signals at the middle of later defined symbol clock signal for storing said digital signals for a symbol clock period,

f) digital comparators responsive to compare said in-phase, negative in-phase, quadrature and negative quadrature signals with a digital value for having digital output signals,

g) digital latches responsive to receive said digital output signals and be sampled by inverted symbol clock for producing synchronized digital output signals,

h) an encoder responsive to multiplex said synchronized digital output signals for producing parallel binary data outputs,

i) logic gates means to select the proper phase error signal form one of said registers by said synchronized digital output signals,

j) a digital carrier loop's low pass filter responsive to receive the selected phase error signal for producing a filtered error compensation digital signal,

k) a digital voltage controlled oscillator responsive to receive said filtered error compensation signal for generating a carrier signal with SIN and COS digital outputs,

l) an exclusive-or gate responsive to receive digital signals from said digital comparators' output for generating a chain of non-overlaping edge signals, and

m) a digital symbol clock regenerator responsive to receive the edge signal form said exclusive-or gate's output for regenerating a symbol clock source.

16. A digital decision-feedback QPSK demodulator defined in claim 15 further comprising the said digital voltage controlled oscillator being a programmable counter with mapped SIN and COS functions outputs.

17. A digital decision-feedback QPSK demodulator defined in claim 15 further comprising means for detecting no output from said digital comparators, disabling the operation of said digital carrier loop's low pass filter and providing the constant output as the last filtered value.

18. A digital decision-feedback QPSK demodulator defined in claim 15 further comprising overlap means responsive for monitoring any time overlaping outputs from said digital latches' outputs which representing a large phase error and selecting a fixed maximum digital value to input of said digital carrier loop's low pass filter.

19. A method of demodulating QPSK signal comprising the steps of aquisiting the phase lock, regenerating the carrier signal and demodulating the data without the requirement of scrambling of input data under normal conditions due to the elimination of imbalance problem between in-phase's and quadrature's error signal.

20. A method according to claim 19, where said regenerating the carrier signal without the imbalance problem includes a selection of correct polarity and in-phase error signal feeding to compensate a voltage controlled oscillator by applying the demodulated data as the decision control.

21. A method according to claim 19, wherein said regenating the carrier signal includes a provision of keeping the said carrier's frequency during blanking of input signal.

22. A method according to claim 19, wherein said step of acquisiting the phase lock includes an acquisition aid by inserting a guarding signal between phase segments to compensate the carrier generator's voltage controlled oscillator and to prevent the slipping of many cycles.

23. A differentially encoded QPSK demodulator comprising:

a) a differentially encoded QPSK modulated input signal.

b) a decision-feedback QPSK demodulator as defined in claim 1, 9 or 15, and

c) a translator means responsive to monitor said

binary data outputs for comparing relative phase change every symbol period and translating back the value of phase change into a decoded binary data.

24. A differentially encoded QPSK demodulator defined in claim 23 wherein said translator means further includes:

a) a first latch for receiving the binary data output from said decision-feedback QPSK demodulator.

b) a comparator for comparing said binary data and the one delayed of one symbol clock from the output of first latch and providing the relative difference as the relative phase change at its output, and

c) a second latch for synchronizing the output of said comparator by the symbol clock.

25. The apparatus of claim 1, 9 or 15 wherein the encoder can be replaced by a reference phase synchronized encoder and further includes:

a) means for detecting and validating a preamble period from said digital outputs,

b) means for extracting a relative position of a reference phase from said digital outputs.

c) means for storing the said relative position during validated preamble period to modulate or adjust the said digital outputs' reference phase, and

d) means for multiplexing said reference phase adjusted digital outputs into a binary encoded data.

Amendments to the claims have been filed, and have the following effect:-

Claims 1-25 above have been deleted.

New or textually amended claims have been filed as follows:-

1. A decision-feedback QPSK demodulator comprising:

a) a first multiplier for producing a product signal of QPSK input signal and a regenerated carrier signal,

b) a second multiplier for producing a product signal of said QPSK input signal and a 90 degrees phase shifted regenerated carrier signal,

c) a first low pass filter responsive to receive said product signal from said first multiplier for producing a filtered in-phase signal,

d) a second low pass filter responsive to receive said product signal from said second multiplier for producing a filtered quadrature signal,

e) a first voltage inverter for inverting said in-phase signal to a negative in-phase signal,

f) a second voltage inverter for inverting said quadrature signal to a negative quadrature signal,

g) sample and hold means responsive to sample said in-phase, negative in-phase, quadrature and negative quadrature signals by a symbol clock signal for holding such said signals at their outputs of a symbol clock period,

h) voltage comparators responsive to compare said in-phase, negative in-phase, quadrature and negative quadrature signals with a potential source for producing digital output signals,

i) digital latches responsive to synchronize said digital output signals from said voltage comparators with said symbol clock signal for producing synchronized digital output signals,

j) an encoder responsive to multiplex said synchronized digital output signals for producing a parallel binary data output,

k) switches responsive to receive output signals from said sample and hold means and be enabled by said synchronized digital output signals for passing a selected phase error signal,

l) a carrier loop low pass filter responsive to receive said selected phase error signal from said switches for producing a filtered error compensation signal,

m) a voltage controlled oscillator responsive to receive said filtered error compensation signal from said carrier loop filter for producing said regenerated carrier signal,

n) an exclusiveor gate responsive to receive said digital output signals from said voltage comparators' outputs for generating a chain of non-overlapping edge pulses, and,

o) a symbol clock regenerator responsive to receive said edge pulses from said exclusive-or gate for regenerating said symbol clock signal.

2. A decision-feedback QPSK demodulator according to claim 1, wherein said first and second low pass filters are a type of integrate-and-dump filter synchronized by said symbol clock signal.

3. A decision-feedback QPSK demodulator as defined in claim 1 or 2 further comprising:

a) means for detecting all low outputs from said voltage comparators, disabling all said switches, and floating input of said carrier loop low pass filter when the input signal being nil, a relative low level one or under a multi-path fading condition, and,

b) said carrier loop filter for latching the last filtered error compensation signal and said voltage controlled oscillator for regenerating the carrier signal with a frequency same as before.

4. A decision-feedback QPSK demodulator according to claim 1 or 2 wherein said output from any voltage comparator is high representing the input of that particular comparator being coherent detected and the sampled output of that voltage comparator is fed to enable a switch having an expected phase error signal input in order to complete the decision-feedback action.

5. A decision-feedback QPSK demodulator according to claim 1, 2 or 4 wherein said coherent detected signal sensed by said voltage comparator's output is 90 degrees laging to said to said expected phase error signal and a proper switch is thus selected according to this relation.

6. A decision-feedback QPSK demodulator as defined in claim 1 or 2 further comprising an overlap detect means responsive for monitoring any time-overlapping output from said digital latches' outputs which representing a large phase error detected, disabling said phase error signal input and enabling a fixed potential source to input of said carrier loop low pass filter.

7. A decision-feedback QPSK demodulator ac-

cording to claim or claim 2 wherein outputs of first and second low pass filters are sampled at the middle of said symbol clock signal to reserve accurate phase difference signals and decision of direction even with large jitter of phase signal input.

8. A decision-feedback demodulator as set forth in claim 6, wherein said enabled fixed potential source acts as a guarding signal between phase segments, intends to limit the acquisition's phase range and expects a fast phase lock acquisition under most conditions.

9. A decision-feedback QPSK demodulator comprising:

a) a first multiplier for producing a product signal of a QPSK input signal and a regenerated carrier signal,

b) a second multiplier for producing a product signal of said QPSK input signal and a 90 degrees phase shifted regenerated carrier signal,

c) a first low pass filter responsive to receive said product signal from said first multiplier for producing a filtered in-phase signal,

d) a second low pass filter responsive to receive said product signal from said second multiplier for producing a filtered quadrature signal,

e) a first voltage inverter for inverting said in-phase signal to a negative in-phase signal,

f) a second voltage inverter for inverting said quadrature signal to a negative quadrature signal,

g) voltage comparators responsive to compare said in-phase, negative in-phase, quadrature and negative quadrature signals with a potential source for producing digital output signals,

h) an encoder responsive to multiplex said voltage compared digital output signals for producing a parallel binary data output,

i) switches responsive to receive output signals from said in-phase, negative in-phase, quadrature and negative quadrature signals and be enabled by outputs of said voltage comparators for passing a selected phase error signal,

j) a carrier loop low pass filter responsive to receive said selected phase error signal for producing a filtered error compensation signal,

k) a voltage controlled oscillator responsive to receive said filtered error compensation signal from said carrier loop low pass filter for producing said regenerated carrier signal,

1) an exclusive-or gate responsive to receive said digital output signals from said voltage comparators' outputs for generating a chain of non-overlapping pulses and,

m) a symbol clock regenerator responsive to receive the said pulses from said exclusive-or gate's output for regenerating said symbol clock signal.

10. A decision-feedback QPSK demodulator according to claim 9, wherein said first and second low pass filters are a type of integrate-and-dump filter synchronized by said symbol clock signal.

11. A decisiion-feedback QPSK demodulator as defined in claim 9 or 10 further comprising:

a) means for detecting no output from said voltage comparators, disabling all said switches, and floating input of said carrier loop low pass filter when the input signal being nil, a relative low level one or under a multi-path fading condition, and,

b) said crrier loop filter for latching the last filtered error compensation signal and said voltage controlled oscillator for generating the carrier signal with a frequency same as before.

12. A decision-feedback QPSK demodulator according to claim 9 or 10 wherein said output from any voltage comparator is high representing the input of that particular comparator being coherent detected and fed to enable a switch having an expected phase error signal input in order to complete the decision-feedback action.

13. A decision-feedback QPSK demodulator according to claim 9, 10 or 12 wherein said coherent detected signal sensed by said voltage comparator's output is 90 degrees laging to said expected error signal and a proper switch is thus selected according to this relation.

14. A decision-feedback QPSK demodulator as defined in claim 9 or 10 further comprising an overlap detect means responsive for monitoring any time-overlapping output from said voltage comparators' outputs which representing a large phase error detected, disabling said phase error signal input and enabling a fixed potential source to input of said carrier loop low pass filter.

15. A decision-feedback QPSK demodulator as set forth in claim 14 wherein said enabled fixed potential source acts as a guarding signal between phase segments, intends to limit the acquisition's phase range and expects a fast phase lock acquisition under most conditions.

16. A decision-feedback QPSK demodulator according to claim 1 wherein the apparatus is in digital form and,

a) said first multiplier is a digital multiplier which contains an analog-to-digital input for producing a digital product signal of said QPSK signal and a digital SIN output of a digitally controlled oscillator,

b) said second multiplier is a digital multiplier which contains an analog-to-digital input for producing a digital product signal of said QPSK signal and a digital COS output of said digitally controlled oscillator,

c) said first and second low pass filters are digital filters,

d) said first and second voltage inverters are digital complementers which produce digital negative value outputs,

e) said voltage comparators are digital magnitude comparators,

f) said sample and hold means are digital registers responsive to sample digital in-phase, negative in-phase, quadrature, and negative quadrature signals from corresponding outputs of said digital filters and digital complementers by said symbol clock signal for storing said digital signals for a symbol clock period,

g) said switches are logic gates for passing a selected digital phase error signal,

h) said carrier loop low pass filter is a digital carrier loop low pass filter,

i) said voltage controlled oscillator is a digitally controlled oscillator responsive to receive said fil-

tered error compensation signal from said digital carrier low pass filter for generating a carrier signal with SIN and COS digital outputs, and,

j) said symbol clock regenerator is a digital symbol clock regenerator.

17. A digital decision-feedback QPSK demodulator defined in claim 9 wherein the apparatus is in a digital form and,

a) said first multiplier is a digital multiplier which contains an analog-to-digital input for producing a digital producing signal of said QPSK signal and a digital SIN output of a digitally controlled oscillator,

b) said second multiplier is a digital multiplier which contains an analog-to-digital input for producing a digital product signal of said QPSK signal and a digital COS output of said digitally controlled oscillator,

c) said first and second low pass filters are digital filters,

d) said first and second voltage inverters are digital complementers which produce digital negative value outputs,

e) said voltage comparators are digital magnitude comparators,

f) said switches are logic gates for passing a selected digital phase error signal,

g) said carrier loop low pass filter is a digital carrier loop low pass filter,

h) said voltage controlled oscillator is a digitally controlled oscillator responsive to receive said filtered error compensation signal from said digital carrier low pass filter for generating a carrier signal with SIN and COS digital outputs, and,

i) said symbol clock regenerator is a digital symbol clock regenerator.

18. A method of demodulating a QPSK signal comprising demodulating and filtering of said QPSK signal into in-phase and quadrature signals with an application of a regenerated carrier signal, selecting an individual correct polarity and in-phase error signal of said in-phase and quadrature signals to an input of a voltage controlled oscillator of a carrier loop via a loop low pass filter by a decision from in digital in-phase data signal, comparing said demodulated in-phase and quadrature signals into digital in-phase data signals, encoding of said compared digital in-phase data signals into a binary parallel data, regenerating said carrier signal from said voltage controlled oscillator and regenerating a symbol clock signal from said digital in-phase data signals.

19. A method according to claim 18 further including keeping the frequency of said regenerated carrier signal constant by floating the input of said loop low pass filter during blanking, a relative low level or a multi-path condition of said QPSK signal.

20. A method according to claim 18 further including speeding the phase lock acquisition by automatically inserting a guarding signal between phase segments to compensate said voltage controlled oscillator and to prevent a slipping of many phase lock cycles.

21. A decision-feedback QPSK demodulator as defined in claim 1 or 9 wherein said QPSK input signal is a differentially encoded QPSK input signal and further comprising a translator means responsive to monitor said binary parallel data output for comparing relative phase change every symbol period and translating back the value of phase change into a differentially decoded data.

22. A decision-feedback QPSK demodulator as defined in claim 16 or 17 wherein said QPSK input signal is a differentially encoded QPSK input signal and further comprising a translator means responsive to monitor said binary parallel data output for comparing relative phase change every symbol period and translating back the value of phase change into a differentially decoded data.

23. A decision-feedback QPSK demodulator as defined in claim 21 or 22 wherein said translator means further includes:

a) a first latch for receiving said binary parallel data output and holding it for a period of said symbol clock signal,

b) a digital comparator for comparing said binary parallel data output and the one delayed of one symbol clock period from the output of said first latch and providing the relative difference as the the relative phase change at its output, and,

c) a second latch for synchronizing the output of said digital comparator by said symbol clock signal as the said differentially decoded data.

24. A decision-feedback QPSK demodulator as defined in claim 1 or 9 wherein said encoder is a referenced phase synchronized encoder and further includes:

a) means for detecting and validating a preamble period from said digital output signals of said voltage comparators,

b) means for extracting a relative position of a reference phase from said digital output signals of said voltage comparators,

c) means for storing said relative position during said validation preamble period to modulate or adjust said digital output signals of said voltage comparators during normal data period, and,

d) means for multiplexing said reference phase adjusted digital output signals into said binary parallel data output.

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